

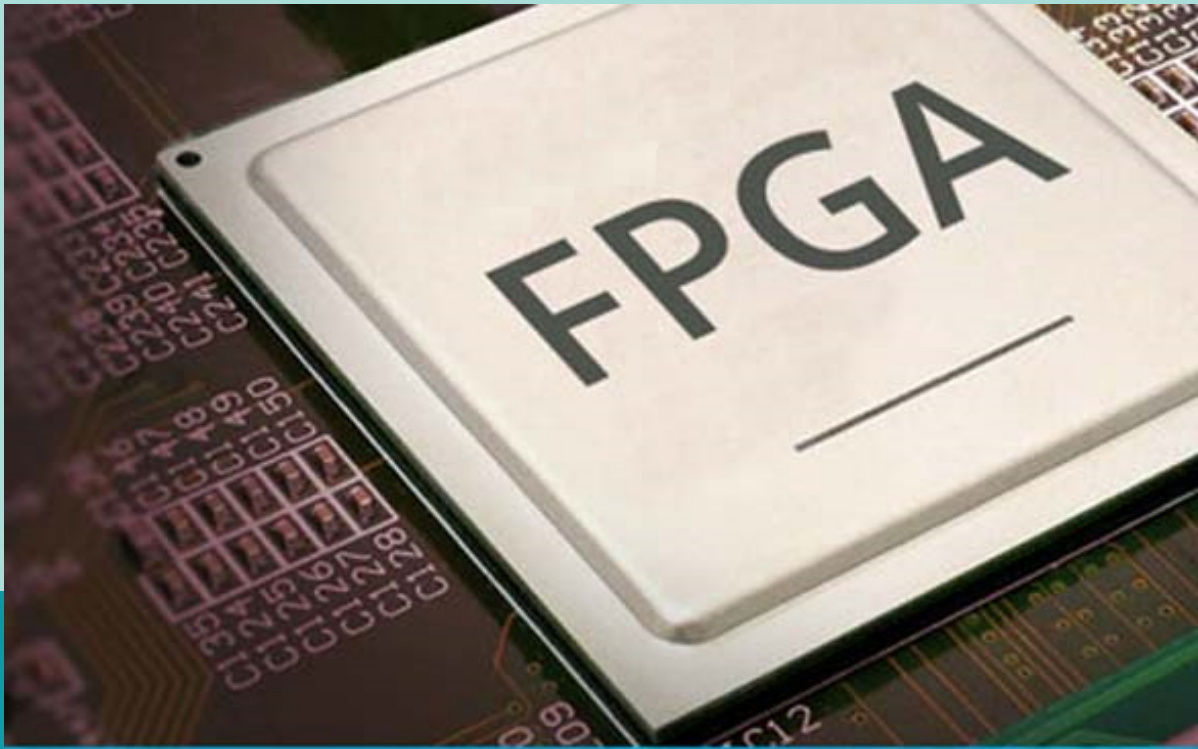


SRI VENKATESWARA COLLEGE OF ENGINEERING
(AUTONOMOUS) - Affiliated to Anna University
Pennalur, Sriperumbudur - 602117



Department of Electrical & Electronics Engineering
Presents

WEBINAR ON
PRODUCT DESIGN PROCESS WITH FPGA



25 May 2020, Mon @6.00pm

An invite for the event will be sent through mail

E - CERTIFICATE WILL BE PROVIDED

Resource Person: Mr. S. Aravind
Senior Engineer
Adani Kattupalli Port Private Limited

Convener :

Dr. KR. Santha

Vice Principal and Head / EEE

SVCE

Co-ordinators:

S. Sinthamani, Asst.Prof / EEE

K.S.Pavithra, Asst.Prof / EEE

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**SRI VENKATESWARA COLLEGE OF ENGINEERING (SVCE)
PENNALUR, SRIPERUMBUDUR-602117**

	Department of Electrical and Electronics Engineering	 INSTITUTION'S INNOVATION COUNCIL <small>(Ministry of HRD Initiative)</small>	 <small>ISO 9001:2015 Certified by IRQS</small> <small>MGMT. SYS. RvA C 071</small>
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REPORT ON Webinar on PRODUCT DESIGN PROCESS WITH FPGA by S. Aravind, Senior Engineer, Adani Kattupalli Port Private Limited.

Date: 25-5-2020

Time: 6.00 pm to 7.45 pm

Objectives (Maximum 50 words):

The main objective of the talk was to give a brief overview of the design steps in using FPGA for a product design- from product idea till burning the code in FPGA board. The design process begins with selecting the mode of design, selecting the programming language (verilog/VHDL), followed by selecting the appropriate FPGA board. These were the topics of interest that was intended to be covered in the talk.

About the programme (Min 500 words):

A Field Programmable Gate Array, or FPGA, is a semiconductor device that comprises of logic blocks which are programmed to execute a specific set of functions. The speaker introduced the basics of microprocessor and microcontroller and then the evolution of FPGA. A comparative case study of FPGA with other programmable devices such as microprocessors/microcontrollers were also discussed.

Then the basic internal architecture of FPGA was briefed. A basic FPGA architecture consists of thousands of fundamental elements called configurable logic blocks (CLBs) surrounded by a system of programmable interconnects, called a fabric, that routes signals between CLBs. Input/output (I/O) blocks interface between the FPGA and external devices. Depending on the

manufacturer, the CLB may also be referred to as a logic block (LB), a logic element (LE) or a logic cell (LC). An individual CLB is made up of several logic blocks. A lookup table (LUT) is a characteristic feature of an FPGA. An LUT stores a predefined list of logic outputs for any combination of inputs: LUTs with four to six input bits are widely used. Standard logic functions such as multiplexers (mux), full adders (FAs) and flip-flops are also common.

The digital logic implementation with these structures was then discussed. Taking a logical expression (Truth table) implemented on SRAM programmed MUX was explained with an example. The different design steps to handle the logic design was explained vividly under 3 main heads- Hardware, software and Programming Language. Hardware - FPGA Development board or custom made product that has FPGA in it with programming peripheral (JTAG) and a JTAG Programmer. The choice the hardware board for a particular design is crucial step. Going through datasheet is very important to know the features available in a particular FPGA. One of the main Hardware constraints that is faced while selecting the FPGA is the number of Logic blocks available in the FPGA. This means that the program written shouldn't require more than the available logic blocks to run. The type of package chosen is very important. Each package of a family of FPGAs varies from one another in certain features like number of GPIOs, availability of memory controller blocks, number slices, Flipflops, size of Distributed RAM, Size and number of Block RAM Blocks, DSP slices, GTP Tranceivers, etc. Software - Programming Environments – They are provided by the manufacturers themselves. Though there are certain 3rd party software to program FPGA, the software provided by the manufacturer has far many options and range of boards. Programming Language – Hardware Description Languages (HDLs) like Verilog HDL and VHDL.

A short demo on how to handle the Xilinx IDE in developing a project, run the code, synthesize the code, develop test bench and simulate the code and finally burn the code in the corresponding hardware was demonstrated by the speaker.

Benefits (Maximum 50 words):

The attendees of this webinar would have gained knowledge on the basic difference between FPGA and other programmable devices like microprocessor and microcontroller, the basic architecture of FPGA, designing a logic circuit using appropriate design steps and finally a fair idea of how to handle Xilinx IDE.

Prepared by Faculty Name, Designation & Dept.

S. Sinthamani, AP/EEE

K.S. Pavithra, AP/EEE

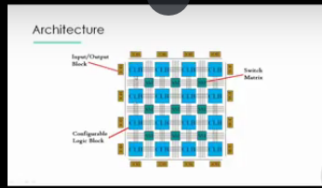


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Co ordinator



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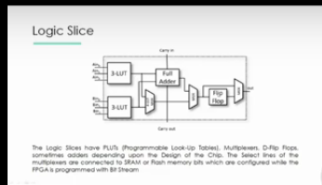


A screenshot of a meeting application interface. At the top, it shows a group of 92 participants. Below this, a list of participants is displayed, each with a circular profile picture and a name. The participants listed are: "SINTHAMANI S EEE (You)", "SINTHAMANI S EEE", "Aravind S", and "Aravind S". Below the list, there is a section for "Others in the meeting (88)".

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A screenshot of a meeting application interface, similar to the one above. It shows a group of 93 participants. The list of participants includes: "SINTHAMANI S EEE (You)", "SINTHAMANI S EEE", "Aravind S", and "Aravind S". Below the list, there is a section for "Others in the meeting (88)".

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